Technical Details

Documentation:
6 Channel Carrier Board for FPD-Link III Cameras with NVIDIA® Jetson™ SoMs

THE IMAGINGSOURCE
TECHNOLOGY BASED ON STANDARDS

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1 Introduction

This carrier board enables the connection of up to six cameras via FPD-Link-III interface to the NVIDIA Jetson SoMs. A powerful on-board 50 watt power converter provides enough power for the SoM and camera modules. The FPD-Link connections are supplied with 18V for compatibility with The Imaging Source's camera modules. The board is available with and without housing.

2 Board Specifications

Physical dimension: 100 mm x 127 mm

Temperature range (board): 0 – 70 °C

2.1 Supported NVIDIA SoMs

NVIDIA Jetson Nano (further referenced as "Nano SoM“ in this document)

NVIDIA Jetson Xavier NX (further referenced as "NX SoM“ in this document)

2.2 Standard Interfaces

1x Gigabit Ethernet (RJ45)

1x USB 3.0 (Nano SoM) / USB 3.2 Gen 2 (NX SoM)

1x USB 2.0

1x USB 2.0 OTG (Micro-USB receptacle)

1x HDMI 2.0a/b

1x display port 1.2a (Nano SoM) / display port 1.4 (NX SoM)

1x SD card (microSD receptacle)

1x barrel jack (2.5 / 5.5 mm) for power supply

2.3 Interfaces Accessible via Screw Terminals or JST PA Connector

2x opto-isolated general-purpose inputs, 3.3V – 36V, max. 12mA @ 36V (screw terminal and JST PA connector)

2x opto-isolated, general-purpose outputs, max. 36V / 100mA (screw terminal and JST PA connector)

1x GND screw terminal

1x power supply via screw terminal

1x external power switch (JST PA connector)

1x external power on signal (screw terminal). Apply a voltage between 5V and 36V to switch the system on/off. This input is not opto-isolated, (see ***Table 2.6*** for possible modes).

1x UART (JST PA connector, RS-232 with RTS/CTS hardware flow control)

1x CAN bus (JST PA connector, NX SoM only)

1x I^2C bus (JST PA connector, 3.3V / 5V)

1x SPI bus (JST PA connector, 1.8V)

1x I2S (JST PA connector, 1.8V)

2.4 Internal Interfaces

1x M.2 slot with key M Size 2280 for NVMe SSDs

1x M.2 slot with key E Size 2230 for Wi-Fi cards

1x fan (PicoBlade connector)

1x DSI display interface (Nano SoM only).

2.5 Buttons

The board has three buttons:

Power button: switches the system on/off.

Depending on the installed OS version and OS configuration, this button can also be used to efficiently shut the system down, put the system into suspend mode, or wake it up again.

Tap the power button: Starts board, puts it to sleep or wakes it up

Press and hold power button for at least 6 seconds: Turns board off without shutting it down.

Reset button: forces a hardware reset.

Recovery button: Press this button together with the ***reset button*** to put the system into "recovery mode". *Please check the NVIDIA Download Center for platform documentation.*

2.6 DIP Switches

There are 6 DIP switches on the back of the board with the following functions:

Switch	Default	Function
1	off	On: The system starts as soon as external power is applied to J2 or J3. The power switch SW2 (or a signal applied to J4 or J5) now only functions to put the system to sleep or to wake it up.
2	off	On: The power state of the system is controlled via an external logic signal applied to J4 or J5. The system is on as long as the logic signal is present. The power button SW2 has no function.
3	off	On: When this switch is on and Switch 2 is off, the system will turn on automatically when the opto-isolated, general-purpose input 1 sees a logic high.
4	off	On: When this switch is on and switch 2 is off, the system will turn on automatically when the opto-isolated, general-purpose input 2 sees a logic high.
5	off	On: The system automatically enters the recovery mode when an USB cable is connected to the OTG port.
6	off	On: Set the voltage level of the external I2C-bus to 3.3V. Off: Set the I2C voltage level to 5V.

3 Connectors and Pinout

Positions of connectors, switches and LEDs

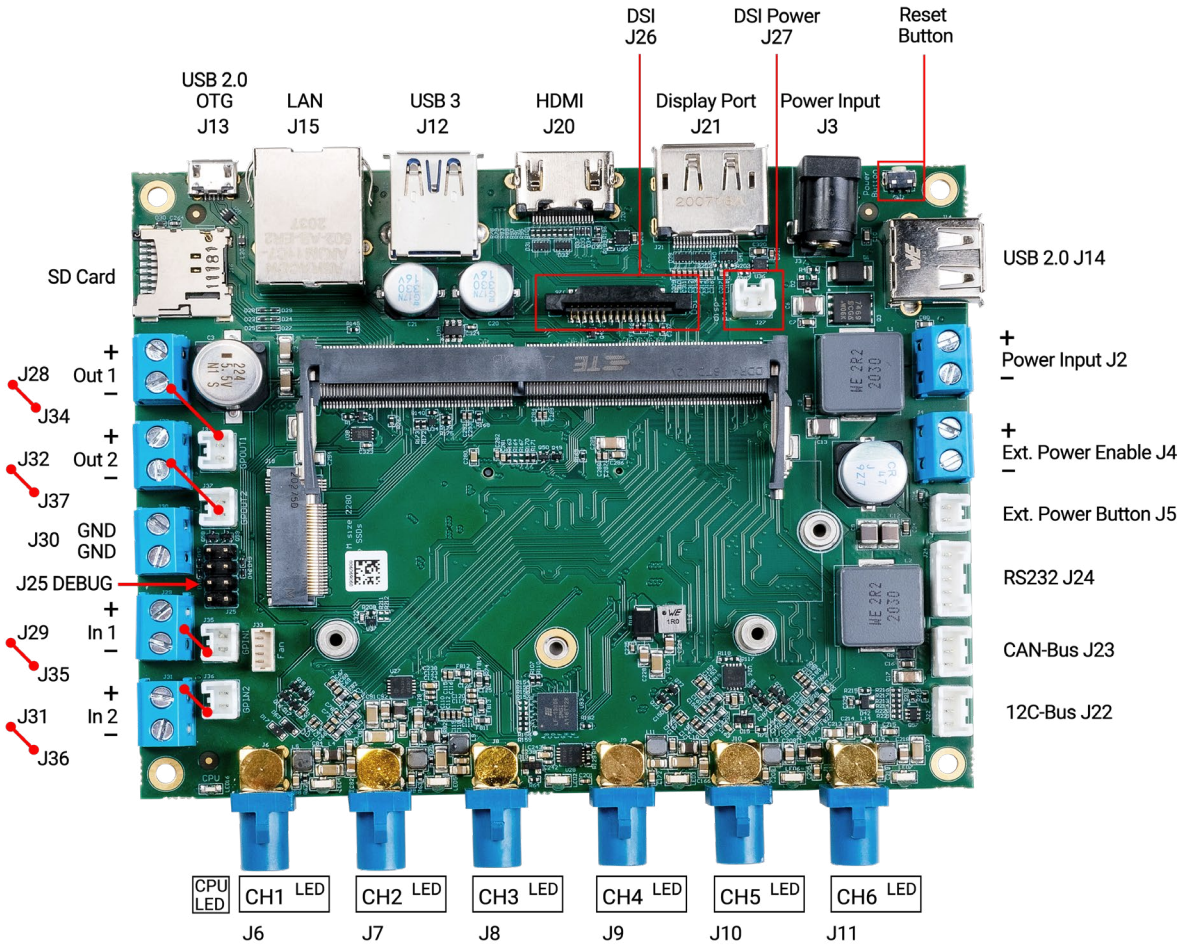

Figure 1. 6 channel carrier board (front view) with connectors and pinout.

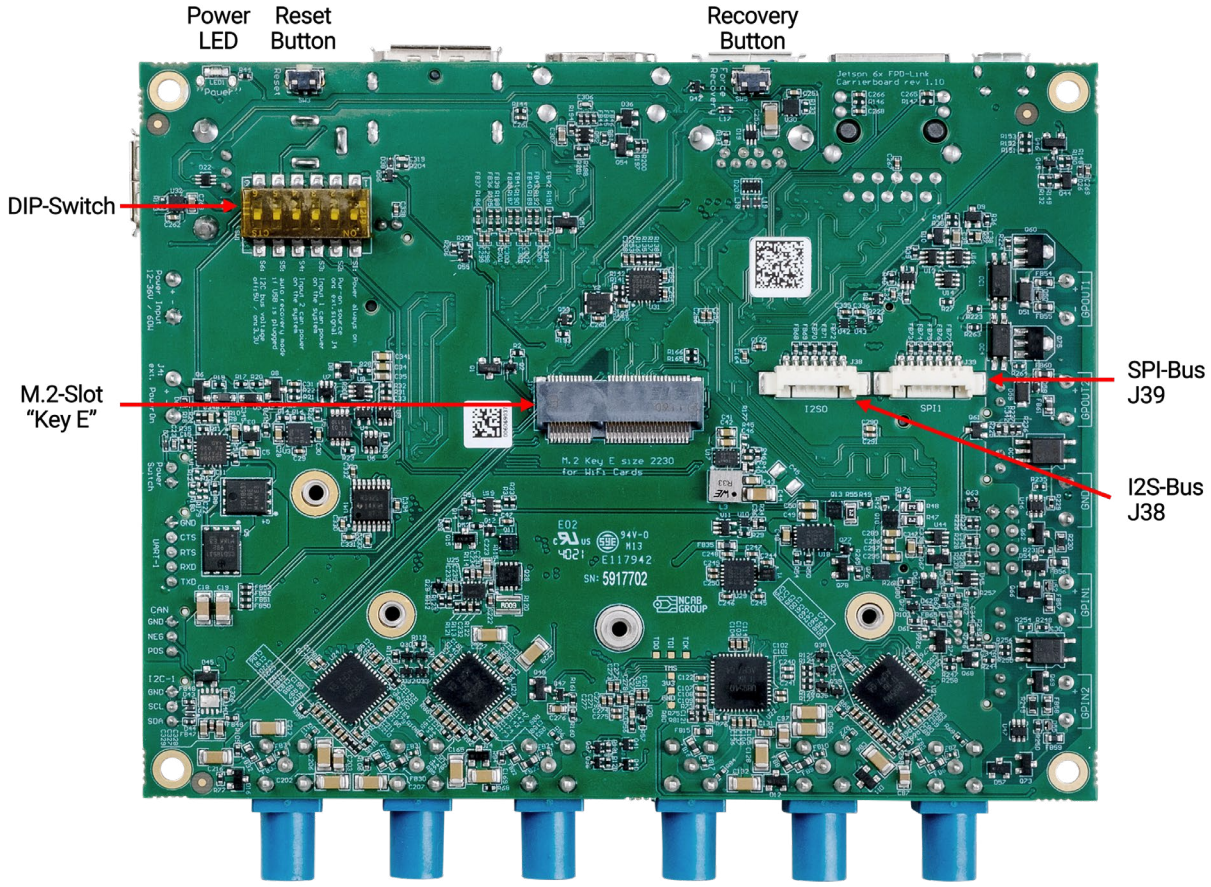

Figure 2: 6 channel carrier board (back view) with connectors and pinout.

3.1 Power Input [J2]

This screw terminal is connected in parallel to the barrel jack, J3.

It provides an alternate way of supplying the board with power.

Pin Number	Default	Description
1	GND	
2	VCC	Supply voltage 12V to 36V, max. 60 Watt

3.2 Power Enable Input [J4]

The function of this screw terminal depends on the configuration of DIP switch 2. When DIP switch 2 is off, this input mimics the behavior of the power-on push-button. If DIP switch 2 is on, the system is on as long as a logic high level is applied to this screw terminal.

Pin Number	Signal Name	Description
1	GND	
2	VCC	Logic signal 5V to 36V, max. 7mA (3.5mA @ 5V) Referenced to system GND!

3.3 Power Button [J5]

An external power switch can be connected to this port.

The part number of the header on the board is B02B-PASK-1 (JST).

Pin Number	Signal Name	Description
1	Power Button	Connect this siganal to GND to switch the system on or off.
2	GND	

3.4 UART / RS-232 [J24]

This connector provides the UART1 interface of the SoM as RS-232 compliant interface with RTS/CTS hardware handshake signals. These signals can be connected directly to a DB9 connector.

The part number of the header on the board is B05B-PASK-1 (JST).

Pin Number	Signal Name	Description
1	GND	System ground / Shield.
2	CTS	Clear to send / Ready to receive (input signal)
3	RTS	Request to send (output signal)
4	RXD	Receive data (input signal)
5	TXD	Transmit data (output signal)

3.5 CAN Bus [J23]

The CAN bus is only available with the Jetson Xavier NX SoM. *Please check the NVIDIA Download Center for platform documentation.* **Note:** The required CAN bus transceiver chip is already on the board, but a terminating resistor is not present.

The part number of the header on the board is B03B-PASK-1 (JST).

Pin Number	Signal Name	Description
1	GND	System ground / Shield.
2	CANL	Low-level CAN bus line
3	CANH	High-level CAN bus line

3.6 I²C Bus [J22]

The I²C bus supports 3.3V and 5V signaling depending on the state of DIP switch 6. It is connected to the I²C1 bus of the SoM.

The part number of the header on the board is B03B-PASK-1 (JST).

Pin Number	Signal Name	Description
1	GND	System ground.
2	SCL	Clock with 1.2k pull-up resistor on board
3	SDA	Data with 1.2k pull-up resistor on board

3.7 Opto-Isolated Input 1 [J29,J35]

The opto-isolated input 1 is available through the screw terminal J29 and the JST header J35. It accepts voltages between 3.3V and 36V, and the input current ranges from 5mA to 12mA. The input can be driven directly from a 3.3V or 5V CMOS digital output pin, and can also be connected directly to a 24V to 36V PLC output. There is no additional series resistor required. Make sure that your voltage source can drive at least a current of 2 mA into the opto-isolated input. However, to reduce current consumption and power dissipation on the board, a series resistor of 1k for 5V or 4.7k for 24V can be used.

The part number of the header on the board is B02B-PASK-1 (JST).

Terminal Pin	JST Pin	Signal Name	Description
1	2	IN2-P	Positive input pin (potential free).
2	1	IN2-N	Negative input pin (potential free)

3.8 Opto-Isolated Input 2 [J31,J36]

The opto-isolated input 2 is available through the screw terminal J31 and the JST header J36. It accepts voltages between 3.3V and 36V, and the input current ranges from 5mA to 12mA. The input can be driven directly from a 3.3V or 5V CMOS digital output pin, and can also be connected directly to a 24V to 36V PLC output. There is no additional series resistor required. Make sure that your voltage source can drive at least a current of 2 mA into the opto-isolated input. However, to reduce current consumption and power dissipation on the board, a series resistor of 1k for 5V or 4.7k for 24V can be used.

The part number of the header on the board is B02B-PASK-1 (JST).

Terminal Pin	JST Pin	Signal Name	Description
1	2	IN2-P	Positive input pin (potential free)
2	1	IN2-N	Negative input pin (potential free)

3.9 Opto-Isolated Output 1 [J28,J34]

The opto-isolated output 1 is available through the screw terminal J28 and the JST header J34. It can switch voltages up to 36V and currents up to 100mA.

The part number of the header on the board is B02B-PASK-1 (JST).

Terminal Pin	JST Pin	Signal Name	Description
1	2	OUT1-P	Positive output pin (potential free)
2	1	OUT1-N	Negative output pin (potential free)

3.10 Opto-Isolated Output 2 [J32,J37]

The opto-isolated output 2 is available through the screw terminal J32 and the JST header J37. It can switch voltages up to 36V and currents up to 100mA.

The part number of the header on the board is B02B-PASK-1 (JST).

Terminal Pin	JST Pin	Signal Name	Description
1	2	OUT2-P	Positive output pin (potential free)
2	1	OUT2-N	Negative output pin (potential free)

3.11 GND Terminal [J30]

This terminal provides system ground on two pins. This GND can be used to convert the opto-isolated inputs and outputs to GND related I/Os.

The part number of the header on the board is B02B-PASK-1 (JST).

Pin Number	Signal Name	Description
1	GND	System ground
2	GND	System ground

3.12 Fan Connector [J33]

A fan can be connected to this port to provide active cooling for the SoM.

The part number of the header on the board is 53047-0410 (Molex PicoBlade).

Pin Number	Signal Name	Description
1	GND	System ground
2	+5V	5V power supply
3	TACHO	Optional tacho input
4	PWM	PWM speed control

3.13 Debug Connector [J25]

The connector used is a 8-pin double row 0.1" pin header.

Pin Number	Signal Name	Description
1	3.3V	3.3V supply voltage
2	5V	5V supply voltage
3	DBG_TXD	Debug UART, TXD signal, 3.3V level
4	RESET	Active high system reset (3.3V - 5V)
5	DBG_RXD	Debug UART, RXD signal, 3.3V level
6	RECOVERY	Active high force-recovery signal (3.3V - 5V)
7	GND	System ground
8	GND	System ground

3.14 DSI Connector [J26]

The DSI connector is only available together with the Jetson Nano SoM.

Pin Number	Signal Name	Description
1	GND	System ground
2	DSI_D1_N	DSI data lane 1
3	DSI_D1_P	DSI data lane 1
4	GND	System ground
5	DSI_CLK_N	DSI clock lane
6	DSI_CLK_P	DSI clock lane
7	GND	System ground
8	DSI_D0_N	DSI data lane 0
9	DSI_D0_P	DSI data lane 0
10	GND	System ground
11	I2C_SCL	I2C clock signal, 3.3V
12	I2C_SDA	I2C clock signal, 3.3V
13	GND	System ground
14	+3.3V	3.3V supply voltage
15	+3.3V	3.3V supply voltage

3.15 FPD-Link Connectors

The board has six FPD-Link III FAKRA connectors with Z-coding.

IMPORTANT: The FAKRA connectors provide a supply voltage of 18V at a maximum current of 250mA. Only connect camera modules from The Imaging Source to these connectors! Otherwise, you could damage the camera module.

When using this carrier board together with the NVIDIA Jetson Nano SoM, some FPD link channels are not available because the Nano SoM does not support MIPI virtual channels:

FAKRA Connector	NVIDIA Jetson Nano SoM	NVIDIA Jetson Xavier NX SoM
CH1	supported	supported
CH2	not available	supported
CH3	supported	supported
CH4	supported	supported
CH5	supported	supported
CH6	not available	supported

4 LEDs

4.1 Power LED

The power LED indicates the power-up status of the system. It is lit when the SoM is active and has activated its peripherals. The LED is not lit if there is no SoM module in the DIMM slot.

4.2 CPU LED

The LED at the far left of the FPD-Link connectors is the CPU LED. It is a yellow LED that is controlled by software. The meaning of this LED is user-defined.

4.3 FPD-Link LEDs

These LEDs show the status of the appropriate FPD-Link channel, which is located at the left side of the LED. These LEDs have three states: If an LED is off, the channel has no power and is not initialized. If an LED is red, the channel is powered but there is no data connection established. If no camera module is connected, this error can be ignored. Otherwise, a red LED indicates a problem with the coaxial cable or the camera module itself. The LED is green when there is a data connection (the camera module is ready or is already streaming video data).

Note: If a camera module is connected and the LED is expected to light green but does not light at all, there may be a short circuit in the FPD-link connection (coaxial cable).

The table shows which LED is controlled by which signal:

LED	Control signal
CH1	Deserializer 1, LOCK and PASS signal
CH2	Deserializer 1, GPIO4 (this LED can also be controlled by the FPGA)
CH3	Deserializer 2, LOCK and PASS signal
CH4	Deserializer 3, LOCK and PASS signal
CH5	Deserializer 4, LOCK and PASS signal
CH6	Deserializer 4, GPIO4 (this LED can also be controlled by the FPGA)

Appendix

5 FPD-Link III Deserializer

There are four FPD-Link III deserializers "DS90UB954" (or compatible) on the board. The following table shows which FPD-Link input is connected to which deserializer. The phantom power supply of the FPD-Link channels must be activated separately for each channel, the corresponding GPIO pin on the deserializer is also listed in the table.

FPD-Link Input	Deserializer	MIPI-Channel at the SoM	Power-Enable Pin on Deserializer
CH1	1 (U21)	CSI0 and CSI1 (2 + 2 MIPI lanes)	GPIO5 (U21 pin 9)
CH2			GPIO6 (U21 pin 8)
CH3	2 (U22)	CSI2 (2 MIPI lanes)	GPIO6 (U22 pin 8)
CH4	3 (U23)	CSI3 (2 MIPI lanes)	GPIO6 (U23 pin 8)
CH5	4 (U24)	CSI4 (4 MIPI lanes)	GPIO5 (U24 pin 9)
CH6			GPIO6 (U24 pin 8)

6 I²C Buses and Devices

The Jetson SoM modules provide a couple of I²C buses. The table below lists the additional I²C devices on the Carrier Board together with the hardware I²C bus and the logical software device name:

I2C Bus	Device Name on Nano SoM	Device Name on NX SoM	I2C Device Address	Description
CAM_I2C	i2c-6	i2c-2	0x30	Deserializer 1
CAM_I2C	i2c-6	i2c-2	0x32	Deserializer 2
CAM_I2C	i2c-6	i2c-2	0x34	Deserializer 3
CAM_I2C	i2c-6	i2c-2	0x36	Deserializer 4
CAM_I2C	i2c-6	i2c-2	0x44	FPGA (register control interface)
I2C0	i2c-0	i2c-1	0x40, 0x43	FPGA (configuration interface)
I2C0	i2c-0	i2c-1	0x48	Temperature sensor TMP100
I2C1	i2c-1	i2c-8	user defined	External I2C bus (via terminal block)
I2C2	i2c-2	i2c-0	0x57	EEPROM AT24C07

Appendix *continued*

7 FPGA

There is an FPGA on the carrier board that provides a connection matrix between the various available inputs and outputs on the board (screw terminals, I/Os at the SoM and I/Os on the four deserializer chips). The FPGA is controlled via an I^2C interface.

The FPGA has the 7-bit I^2C-address 0x44 and is connected to the camera I^2C bus on the SoM (CAM_I2C). The register interface is very simple: To write to a register in the FPGA, send the 8-bit register address followed by the 8-bit data to be written to the register. To read a register, first send the 8-bit register address and then initiate a new I^2C read transfer to read the 8-bit data from the register.

List of implemented registers:

Register	Read / Writer	Description
0x00	R	Board revision number
0x01	R/W	Deserializer control register: Bit 0 : set to 1 to force a hardware reset of the deserializer. 0 = normal operation. Bit 1-7 : reserved
0x02	R/W	GPIO (via terminal blocks) - control and status registers Bit 0 : 0 = GPOUT1 controlled by global multiplexer, 1 = GPOUT1 controlled by bit 1 of this register Bit 1 : 0 = set GPOUT1 high impedance, 1 = set GPOUT1 to conducted mode Bit 2 : 0 = GPOUT2 controlled by global multiplexer, 1 = GPOUT2 controlled by bit 3 of this register Bit 3 : 0 = set GPOUT2 high impedance, 1 = set GPOUT2 to conducted mode Bit 4 : status: current state of GPOUT1 Bit 5 : status: current state of GPOUT2 Bit 6 : status: current state of GPIN1 Bit 7 : status: current state of GPIN2
0x03	R/W	set source for signal on GPOUT1 (terminal block)
0x04	R/W	set source for signal on GPOUT2 (terminal block)
0x05	R/W	set source for signal on SOC pin GPIO01
0x06	R/W	set source for signal on SOC pin GPIO04
0x07	R/W	set source for signal on SOC pin GPIO07
0x08	R/W	set source for signal on SOC pin GPIO10
0x09	R/W	set source for signal on SOC pin GPIO11
0x0A	R/W	set source for signal on SOC pin GPIO13
0x0B	R/W	set source for signal on deserializer 1 pin GPIO0
0x0C	R/W	set source for signal on deserializer 1 pin GPIO1
0x0D	R/W	set source for signal on deserializer 1 pin GPIO2

Appendix *continued*

Table of implemented registers continued

Register	Read / Writer	Description
0x0E	R/W	set source for signal on deserializer 1 pin GPIO3
0x0F	R/W	set source for signal on deserializer 1 pin GPIO4
0x10	R/W	set source for signal on deserializer 2 pin GPIO0
0x11	R/W	set source for signal on deserializer 2 pin GPIO1
0x12	R/W	set source for signal on deserializer 2 pin GPIO2
0x13	R/W	set source for signal on deserializer 2 pin GPIO3
0x14	R/W	set source for signal on deserializer 2 pin GPIO4
0x15	R/W	set source for signal on deserializer 3 pin GPIO0
0x16	R/W	set source for signal on deserializer 3 pin GPIO1
0x17	R/W	set source for signal on deserializer 3 pin GPIO2
0x18	R/W	set source for signal on deserializer 3 pin GPIO3
0x19	R/W	set source for signal on deserializer 3 pin GPIO4
0x1A	R/W	set source for signal on deserializer 4 pin GPIO0
0x1B	R/W	set source for signal on deserializer 4 pin GPIO1
0x1C	R/W	set source for signal on deserializer 4 pin GPIO2
0x1D	R/W	set source for signal on deserializer 4 pin GPIO3
0x1E	R/W	set source for signal on deserializer 4 pin GPIO4
0x1F	R/W	set source for CPU LED signal
0x20	R	Status of SOC GPIOs Bit 0 : GPIO01 Bit 1 : GPIO04 Bit 2 : GPIO07 Bit 3 : GPIO10 Bit 4 : GPIO11 Bit 5 : GPIO13 Bit 6-7 : reserved
0x21	R	Status of deserializer 1 GPIOs Bit 0 : GPIO0 Bit 1 : GPIO1 Bit 2 : GPIO2 Bit 3 : GPIO3 Bit 4 : GPIO4 Bit 5-7 : reserved

Appendix *continued*

Table of implemented registers continued

Register	Read / Writer	Description
0x22	R	Status of deserializer 2 GPIOs Bit 0 : GPIO0 Bit 1 : GPIO1 Bit 2 : GPIO2 Bit 3 : GPIO3 Bit 4 : GPIO4 Bit 5-7 : reserved
0x23	R	Status of deserializer 3 GPIOs Bit 0 : GPIO0 Bit 1 : GPIO1 Bit 2 : GPIO2 Bit 3 : GPIO3 Bit 4 : GPIO4 Bit 5-7 : reserved
0x24	R	Status of deserializer 4 GPIOs Bit 0 : GPIO0 Bit 1 : GPIO1 Bit 2 : GPIO2 Bit 3 : GPIO3 Bit 4 : GPIO4 Bit 5-7 : reserved
0x25	R	Bit 0 : CPU LED status, Bit 1-7 : reserved
0x3F	R	FPGA version number

Appendix *continued*

Below, please find a list of all available source signals that can be used for the various outputs.

To connect an output to a specific source, simply write one of these values into one of the registers 0x03 to 0x1F:

Value	Source Signal (or Fixed Output Signal)
0x00	Set the pin to input mode (high-Z with weak pull-up), do not output anything on this pin
0x01	Drive a constant '0'
0x02	Drive a constant '1'
0x03	GPIN 1 (terminal block)
0x04	GPIN 2 (terminal block)
0x05	SOC GPIO01
0x06	SOC GPIO04
0x07	SOC GPIO07
0x08	SOC GPIO10
0x09	SOC GPIO11
0x0A	SOC GPIO13
0x0B	Deserializer 1 GPIO0
0x0C	Deserializer 1 GPIO1
0x0D	Deserializer 1 GPIO2
0x0E	Deserializer 1 GPIO3
0x0F	Deserializer 1 GPIO4
0x10	Deserializer 2 GPIO0
0x11	Deserializer 2 GPIO1
0x12	Deserializer 2 GPIO2
0x13	Deserializer 2 GPIO3
0x14	Deserializer 2 GPIO4
0x15	Deserializer 3 GPIO0
0x16	Deserializer 3 GPIO1
0x17	Deserializer 3 GPIO2
0x18	Deserializer 3 GPIO3
0x19	Deserializer 3 GPIO4
0x1A	Deserializer 4 GPIO0
0x1B	Deserializer 4 GPIO1
0x1C	Deserializer 4 GPIO2
0x1D	Deserializer 4 GPIO3
0x1E	Deserializer 4 GPIO4
0x1F	reserved

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All weights and dimensions are approximate. Unless otherwise specified the lenses shown in the context of cameras are not shipped with these cameras.